KUMAR SOUBHAGYA BEHERA

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CAREER OBJECTIVE

Hard working and passionate job seeker with strong organizational skills. Eager to secure entry level job as an Engineer and ready to help team and achieve company goal. I am enthusiastic, workaholic and eager to contribute to team and success through my skills, hard work and smart work. I am also motivated to learn, grow and excel in industry.

EDUCATION

Malaviya National Institute Of Technology, Jaipur — Aug 2024 – June 2026
Master of Technology - VLSI Design — Jaipur, India
CGPA - 8.39

Parala maharaja Engineering College, Berhampur — Dec 2020 – May 2024
Bachelor Of Technology - Electronics and Telecommunication Engineering — Berhampur, India
CGPA - 8.58

Kendriya Vidyalaya Khordha Road — Apr 2019 – Mar 2020
Intermediate — khordha, India
Percentage - 86.67%

Kendriya Vidyalaya Khordha Road — Apr 2017 – Mar 2018
Matriculation — Khordha, India
Percentage - 93.2%

PROJECT

Design and Implementation of Asynchronous AER Circuit Design for Neuromorphic Chips
Verilog HDL, Neuromorphic Computing, Asynchronous Digital Design, FPGA (Basys-3)

- Studied and implemented asynchronous Address Event Representation (AER) circuits for neuromorphic communication systems.
- Designed mask-based arbitration logic and dual-level AER architecture to reduce latency and hardware area.
- Simulated and verified the design using Verilog HDL, implemented on FPGA (Basys-3) to check the design performance.

FPGA-Based Image Processing System
Verilog HDL, Xilinx Vivado, FPGA (Basys-3), VGA Interface

- Designed and implemented an image processing system on FPGA using Verilog HDL.
- Developed RTL modules for image memory (BRAM), address generation, processing core, and VGA display controller.
- Implemented image enhancement techniques such as Brightness enhancement, grayscale conversion, image inversion, thresholding, red-channel extraction .
- Verified functionality through simulation and deployed the design on FPGA hardware for real-time image display.

FSM-Based Automatic Vending Machine System
Verilog HDL, Xilinx Vivado, Finite State Machine (FSM),

- Designed and implemented a automatic vending machine system using Verilog based on finite state machine (FSM) modeling.
- Accepted predefined coin denominations, developed logic for product dispensing, change reuse, and invalid input handling.
- Designed and simulated the system in Xilinx Vivado

Schematic and Layout Design of CMOS Digital Circuits
Cadence Virtuoso, 180nm Technology, CMOS Design

- Designed and simulated schematic and layout of basic digital building blocks using Cadence Virtuoso.
- Implemented CMOS circuits for Inverter, Flip-Flop (SR, D), and logic gates (AND, OR, NAND, NOR, XOR).
- Performed simulatiom, DRC (Design Rule Check), LVS (Layout vs. Schematic), and area estimation to validate physical design accuracy.

TRAININGS/INTERNSHIPS

BSNL-Regional Telecom Training Centre — Jun 2023 – Jul 2023
6 weeks internship on “ADVANCE TELECOM” — Bhubaneswar, India

Parala Maharaja Engineering College — Jan 2023 – Feb 2023
1 month internship on “VLSI Design using EDA Tools” — Berhampur, India

TECHNICAL SKILLS

- Topic-wise Skills :-Digital Electronics, Digital System Design, Analog layout design
- Software Skills :- Xilinx Vivado , Cadence Virtuoso , MATLAB
- Programming languages :- Verilog HDL, C++
- Other skills :- MS Word , MS Excel , Problem Solving ,Management skills , Good Communication, Leadership

ACHIEVEMENTS

- Got bronze medal in mathematics olympiad
- Positioned top 10 in regional science project exhibition

LANGUAGES

- English
- Hindi
- Odia

STRENGTH

- Hard working
- Responsible
- Good listener
- Quick learner